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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,214	GAMINI ET AL.	
	Examiner	Art Unit	
	Pho M. Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-15* is/are allowed.

6)☒ Claim(s) *2,3,6,7 and 11* is/are rejected.

7)☒ Claim(s) *4,5 and 8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

1. Acknowledgment is made of applicant's Preliminary Amendment filed 28 June 2004. The changes and remarks disclosed therein were considered.

2. Claim 1 has been canceled.

3. Claims 2-15 are pending in the application.

Information Disclosure Statement

4. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 30 December 2003. The information disclosed therein was considered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 2-3, 6-7 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Zandman et al. (US. 2001/0016369).

Regarding independent claim 2, Zandman et al in Figure 1 and Figure 8A-B discloses an integrated circuit package (100, Figure 1) comprising:

a semiconductor substrate (inherence, 116, Figure 8B) including a set of semiconductor devices (semiconductor device 100 which contain separated of the device such as 100A, 100B...100N, Figure 1) separated by one or more interior scribe lane (each of separated device such as 100A, 100B...100N separated by scribe lines 108 and 110, Figure 1, see column 2, paragraph 0020) and

an interconnect channel (connection source pad 106S, gate pad 106G, Figure 1 and Figure 8A are in electrical contact with the gate and source terminal, respectively, of the power with semiconductor device 100A, 100B...100N) extending across the one or more interior scribe lanes to electrically connect at least two semiconductor device (see column 2, paragraph 0020).

With respected to dependence claim 6, Zandman et al in Figure 1 and Figure 8B disclosed the interconnect channel (106S, 106G) includes metal traces (116).

Regarding independent claim 3 and independent claim 7. Zandman et al in Figure 1 and Figure 8A-B discloses an integrated circuit package (100, Figure 1) comprising:

a semiconductor substrate (inherence, 116, Figure 8B) including a set of semiconductor devices (semiconductor device 100 which contain separated of the device such as 100A, 100B...100N, Figure 1) separated by one or more interior scribe lane (each of separated device such as 100A, 100B...100N separated by scribe lines 108 and 110, Figure 1, see column 2, paragraph 0020) wherein at least one semiconductor device is electrically connected to a device bond pad formed on the

semiconductor substrate (connection source pad 106S, gate pad 106G, Figure 1 and Figure 8A are in electrical contact with the gate and source terminal, respectively, of the power with semiconductor device 100A, 100B...100N);

an interconnect (106S, 106G, Figure 1) substrate positioned on the semiconductor substrate (inherence, 116, Figure 8B) and including a substrate bond pad wherein a bond wire electrically connects the device bond pad and the substrate bond pad (connection source pad 106S, gate pad 106G, Figure 1 and Figure 8A are in electrical contact with the gate and source terminal, respectively, of the power with semiconductor device 100A, 100B...100N) and

an interconnect channel (connection source pad 106S, gate pad 106G, Figure 1 and Figure 8A are in electrical contact with the gate and source terminal, respectively, of the power with semiconductor device 100A, 100B...100N) disposed in the interconnect substrate and extending across the one or more interior scribe lanes to electrically connect at least two semiconductor device (see column 2, paragraph 0020).

With respected to dependence claim 11, Zandman et al in Figure 1 and Figure 8B disclosed the interconnect channel (106S, 106G) includes metal traces (116).

Allowable Subject Matter

7. Claims 4-5, 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 4 and 8, the prior art of record do not disclose or suggest the bond ball for bonding the integrated circuit package to a printer circuit board.

Regarding claim 5 and 10, the prior art of record do not disclose or suggest the interconnect substrate includes flexible tape.

Regarding claim 9, the prior art of record do not disclose or suggest an impedance matching device connect to the bus interface for matching an external bus impedance within a predetermined target range.

9. Claims 12-15 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "the method of interconnecting integrated circuit device including the cutting the wafer along selected scribe lane so that the grouped functional device remain interconnected by the interconnect channel" as claimed in the independent claim 12.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kim et al. (US. 6,594,818) disclosed the memory units separated by scribe lane with different storage capacity and cutting edge in the wafer.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PML
31 March 2005

VAN THU NGUYEN
PRIMARY EXAMINER